2017 ES4 Introduction to Digital Logic Circuits

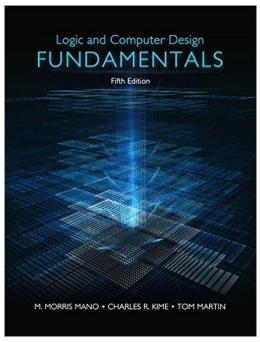
Class webpage available on Trunk

A Link to the Trunk site will also be emailed to all enrolled students

Descriptions and Goals:

Welcome to the world of digital design! Today, every electronic device uses digital electronics. Digital Electronics enable everything from wireless communications to self-driving cars to be realized. In this course, you will be learning all aspects of digital system design and implementation methods. Designing digital systems today has its own set of challenges. Digital designs can be so small that we have to worry about how to test them, how to power them and how to protect them from being used for malicious purposes. To enforce the theoretical concepts, we will use hardware description languages (HDLs) such as the VHDL/Verilog languages to model and simulate designs. Topics we will cover, include number systems, codes and conversions. Two's complement representation. Boolean algebra and Karnaugh map minimization of Boolean expressions. We will then investigate logic gates and implement useful designs in the laboratory using SSI, MSI and LSI logic components. After covering combinational logic, we will introduce flip-flops as memory devices, their characteristics and sequential circuit design including state machines. The course includes a **MANDATORY** hands-on laboratory, where every student will be actively involved and participating in design, simulation, implementation, reporting, writing and making oral presentations, as well as evaluating their teammates contributions and performance. All students must pass the lab component of the class to pass the class.

Prerequisites: you must have taken and passed ES3 Circuit Theory.



Textbook:

Logic and Computer Design Fundamentals
M. Morris Mano, Charles Kime and Tom Martin
ISBN-13: 978-0133760637
ISBN-10: 0133760634
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References:

- "Fundamentals of Digital Logic with VHDL Design", by Stephan Brown and Zvonko Vranesic. The publisher is McGraw Hill.
- "Introduction to Digital Logic Design", John Hayes, Addison Wesley, Reading, MA.

Instructor: Dean, Dr. Karen Panetta

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Office Hours: Tuesday 1:30-3:30pm

Dean Panetta also takes appointments for meetings with students through her staff administrator. Ms. Donna Carriker, room 109E Anderson Hall,
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Head Teaching Assistant:

Mr. Srijith Rajeev <srijith2311@gmail.com> and
Mr. Shishir Rao <shishirprao@gmail.com>
TA: Office Hours: TBD

Specific Topics:

1. Introduction to embedded system design of computers and applications.
2. Binary Systems, bits, base transformations (2 classes).
3. AND, OR, NOT functions, truth tables, gates. (2)
4. Alphanumeric codes, radix arithmetic.
5. 2's complement representation. (2)
6. Booelan theorems, algebraic simplification. (2)
7. Functions, complements, duals, canonical forms.(2)
8. Minterms, maxterms, Sum of Products, Product of Sums , (2)
9. NAND,NOR,XOR,XNOR gates, parity, gates with more than 2 inputs. (2)
10. Karnaugh Maps (3)
11. NAND, NOR implementations, bubble manipulations. (2)
12. Don't cares on K-maps, prime and essential prime implicants (2)
13. MSI combinatorial functions, multiplexor and decoders. (2)
14. Introduction to sequential circuits. (1)
15. SR, D, JK flip-flops, edge-triggered. (2)
16. Counter design using flip-flops.(1)
17. Moore and Mealy machines (3)

Assessment of accomplishments:

- Mastering the material in this course is measured by:
- Quizzes
- Homework
- Laboratory sessions
- A midterm and final examination.

Each of these assessments is discussed in the following sections.

Quiz: There will be a quiz given every Wednesday. The best of FIVE quiz grades will be used. **No make-up quizzes will be given.**

Homework: There will be a homework assignment due every Monday at the **beginning** of class. Homework assignments are posted via Trunk. It is your responsibility to retrieve the homework assignment each week. Solutions to the homework will also be posted on Trunk the day after the due date. All handouts given in class will also available on Trunk. Please scan in all your homework and complete lab reports and keep a pdf copy for yourself.

No late homework will be accepted. If you cannot make class, scan in your homework and email it as a pdf file to Srijith before the deadline.

Collaboration is allowed and encouraged on homework. However, all students involved in collaboration must include the names of all collaborators at the top of their homework assignments. Failure to do so, will be considered plagiarism and will receive no credit.

Calculators or other electronic devices are not allowed for any quiz or exam. It is strongly suggested that when doing the homework, you make sure you can do the problems without use of the calculator, since they will not be available during quizzes or exams.

Lab: There will be five labs consisting of design, hardwired implementation and Simulation.

- Students will sign up for a specific lab session. If you need to attend a different lab section due to illness, you must **pre-arrange** a time with the Teaching Assistant **before** your scheduled lab time. More information on lab requirements will be passed out next week.
- If a pre-lab is required for a lab, then the **Pre-lab will count** as a homework assignment that must be completed before you attend your scheduled lab section.
- Each student will conduct and individual lab and submit an individual lab report that is the unique work of the student.
- **YOU MUST PASS THE LAB COMPONENT OF THE COURSE with a 70% or better OR YOU WILL FAIL THE COURSE**.
- All VHDL/Verilog program code and lab reports are to be the product of a single individual and not collaboration.
- The labs may also have an exit quiz that will count toward each lab report grade.
- There will also be a final project. The final project will require all students make an oral presentation as well as contribute to evaluating their peers' contributions and performance.

Please refer to the complete and detailed laboratory guidelines for ES4.

Examinations: There will be one hour-exam and one final exam. The midterm exam will be given in class on: **Wednesday, March 15, 2017**. The final exam will be announced

according to the university schedule. If you have a schedule conflict for the hourly exam time for some unexpected reason, please get in touch with Dean Jennifer Stephan.

- **In Class attendance/presentation/professionalism:**
  No Electronic devices such as laptops, cell phones, tablets, recording devices or other electronic devices can be used during class time. All devices must be off and stored out of sight. This is to ensure that students in the class are not distracted from paying attention to the lecture. ***Please see the referenced paper:*** *The Pen Is Mightier Than the Keyboard: Advantages of Longhand Over Laptop Note Taking by Pam A. Mueller and Daniel M. Oppenheimer*, should you need more information on the intention of this policy.

- 5 additional bonus points will be added to the final exams of students who are present when randomly called upon anytime during the semester. If a student cannot make a class, professional courtesy requires a message to the instructor from a student indicating that they will not be present. **A70% average in lab work and projects is mandatory.**

Course Grading:

Homework Average:	10%
Project	10%
Quizzes	10%
Lab	25% (**must pass with a 70% or better or final class grade is F.**)
First hour-exam	20%
Final Exam	25%

Incomplete grades will not be given for failure to fulfill class requirements.